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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,658	10/11/2001	Russell Alan Resnick	RPS920010099US1	8633

28722 7590 04/19/2004

BRACEWELL & PATTERSON, L.L.P.
P.O. BOX 969
AUSTIN, TX 78767-0969

EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	4

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,658	RESNICK, RUSSELL ALAN	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16* is/are allowed.

6)☒ Claim(s) *1-3, 5-7, and 9-10* is/are rejected.

7)☒ Claim(s) *4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachm nt(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-7, and 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al.('014), hereinafter referred to as Nguyen.

3. Regarding claim 1, Nguyen discloses an interface circuitry for connecting a data storage device to a computer(Column 3 Lines 64-66), said interface circuitry comprising: a parallel data line for transferring parallel data between the data storage device and the computer; a multi-mode, parallel/serial data line for selectively transferring parallel or serial data between the data storage device and the computer(Column 3, Lines 51-56); a switching circuit, connected to said parallel/serial data line, having first and second selectable modes of operation, said switching circuit being connectable to the computer(Column 4, Lines 5-11); and a data transfer mode selection circuit connected to said switching circuit, said mode selection circuit for sending a parallel mode selection signal to said switching circuit for placing said switching circuit in said first mode of operation, wherein parallel data is transferable between the storage device and the computer over both the parallel data line and the parallel/serial data line, said mode selection circuit for sending a serial mode selection signal to said switching circuit for placing said switching circuit in said second mode of operation, wherein serial data is transferable between

the storage device and the computer over said parallel/serial data line(Column 3, Lines 54-56, Lines 59-61; Column 4, Lines 5-11).

4. Regarding claim 2, Nguyen discloses an interface circuitry, wherein the interface circuitry is electrically connected to an Advanced Technology Attachment/Integrated Drive Electronics (ATA/IDE) bus in the computer(Column 3, Line 44).

5. Regarding claim 3, Nguyen discloses an interface circuitry, wherein the data transfer mode selection circuit is electrically connected to the switching circuit through the ATA/IDE bus(Figure 2).

6. Regarding claim 5, Nguyen discloses an interface circuitry, wherein the data transfer mode selection circuit is electrically connected to the switching circuit via a conductor, oriented between the computer and the data storage device, that is non-dedicated to the data transfer mode selection circuit(Figure 2).

7. Regarding claim 6, Nguyen discloses a computer comprising: a central processing complex (CPC) including a central processing unit(Figure 1, 19), a memory(Figure 1, 18) and a memory and Input/Output (I/O) controller(Figure 1, 14); a data storage device(Figure 2, 21); an interface circuitry coupled between said data storage device and said CPC(Column 3, Lines 64-66), said interface circuitry including: a parallel data line for transferring parallel data between said data storage device and said CPC; a multi-mode, parallel/serial data line for selectively transferring parallel or serial data between the data storage device and said CPC(Column 3, Lines 51-56); a switching circuit, connected to said parallel/serial data line, having first and second selectable modes of operation(Column 4, Lines 5-11); and a data transfer mode selection circuit connected to said switching circuit, said mode selection circuit for sending a parallel mode selection signal to said switching circuit for placing said switching circuit in said first mode of operation, wherein parallel data is transferable between the storage device and

said CPC over both the parallel data line and the parallel/serial data line, said mode selection circuit for sending a serial mode selection signal to said switching circuit for placing said switching circuit in said second mode of operation, wherein serial data is transferable between said storage device and said CPC over said parallel/serial data line(Column 3, Lines 54-56, Lines 59-61; Column 4, Lines 5-11).

8. Regarding claim 7, Nguyen discloses a computer, wherein the interface circuitry is electrically connected to an Advanced Technology Attachment/Integrated Drive Electronics bus(Column 3, Line 44).

9. Regarding claim 9, Nguyen discloses a computer, wherein the data transfer mode selection circuit is electrically connected to the switching circuit through the interface circuitry(Figure 2).

10. Regarding claim 10, Nguyen discloses a computer, wherein the data transfer mode selection circuit is electrically connected to the switching circuit via a conductor, oriented between the computer and the data storage device, that is non-dedicated to the data transfer mode selection circuit(Figure 2).

Allowable Subject Matter

11. Claims 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest a docking station to be connected to the interface circuitry.

12. Claims 11-16 are allowed for the reasons stated in the previous paragraph.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited disclose art related to serial and parallel data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
April 13, 2004

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100